

Dependability in Massively Defective Nanoscale Multicore Processor Architectures

Piotr Zając, Jacques Collet, Yves Crouzet and Jean Arlat
[firstname.lastname@laas.fr]



53rd IFIP WG10.4 Meeting, Natal, Brazil
Research Report Session — Monday February 25, 2008

How did we get where we stand today?

■ Technology improvements:

- ◆ Transistor size ↘; Power supply ↘; Clock frequency ↗; MIPS ↗; ...

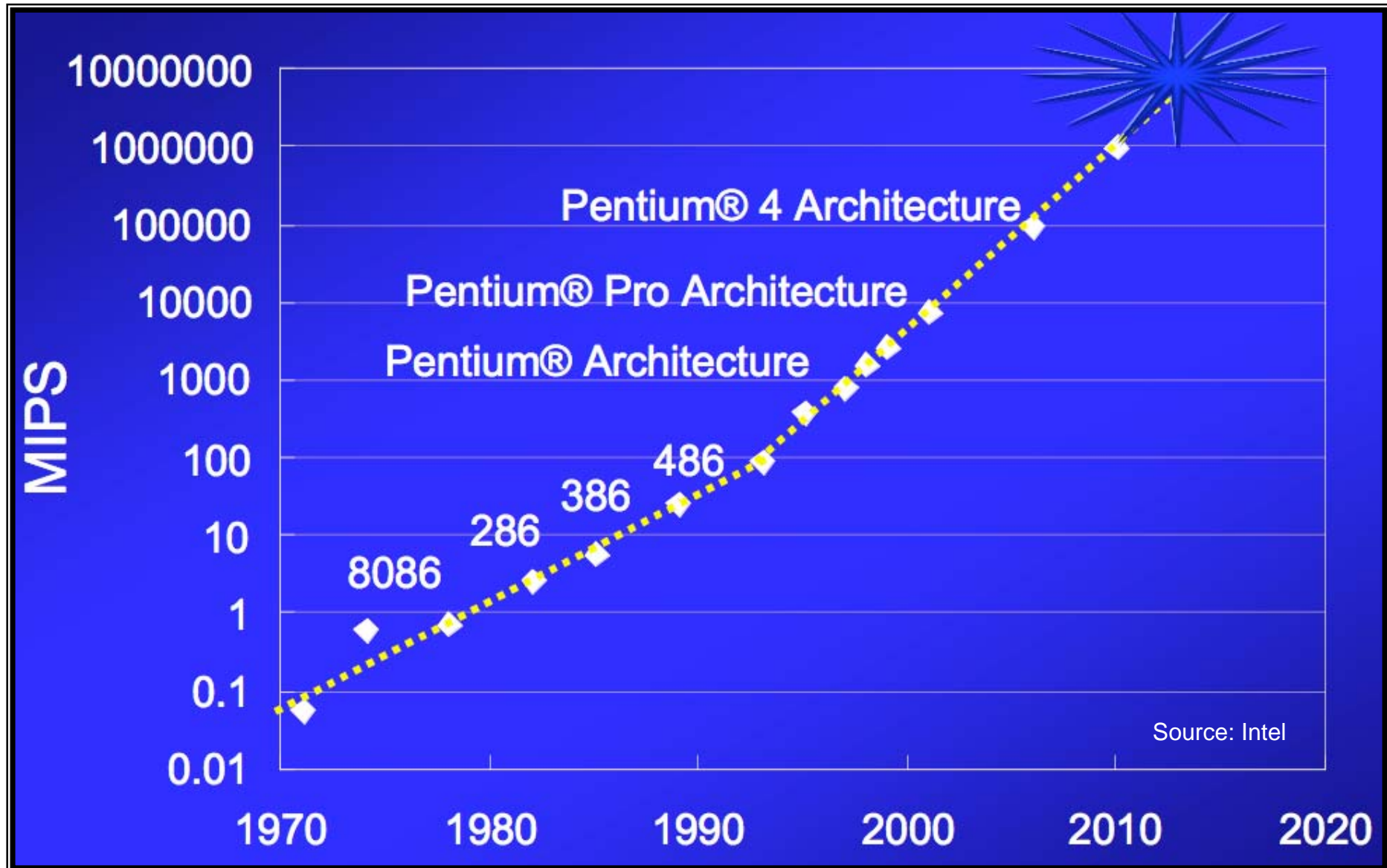
■ Architectural enhancements in processor design:

- ◆ RISC Scalar Architecture, Pipelining & On-die caching (Intel386, AIM PowerPC ...)
- ◆ RISC Super Scalar architecture (“multi-pipelining” and several ALUs/FPUs) and Branching prediction (Intel Pentium, AIM PowerPC970,...)
- ◆ “Out-of-order” instruction processing — a form of data flow operation (Intel Pentium Pro, Power PC, etc.)
- ◆ Extended pipelining stages (up to 20) introduction of execution trace cache and hyper-threading (Intel Pentium 4)

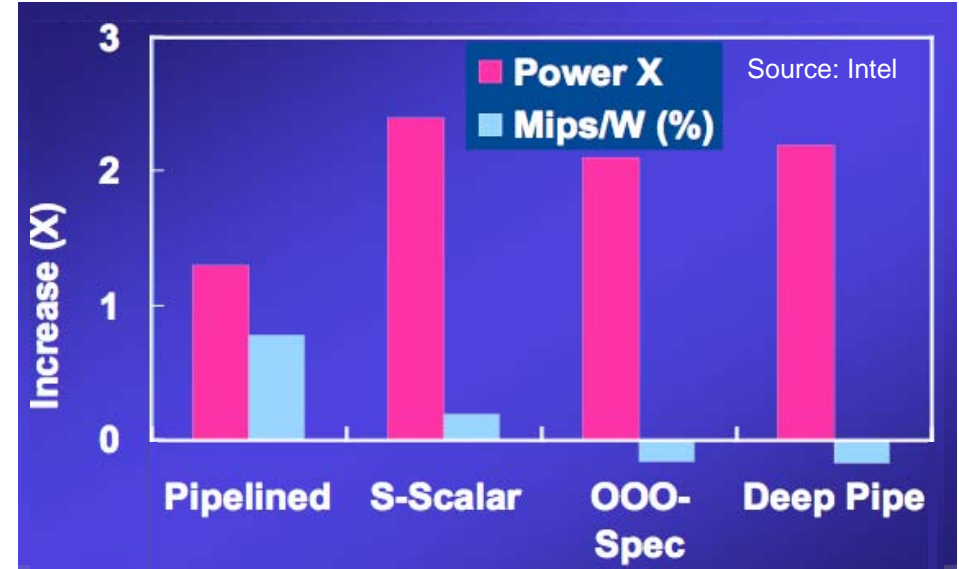
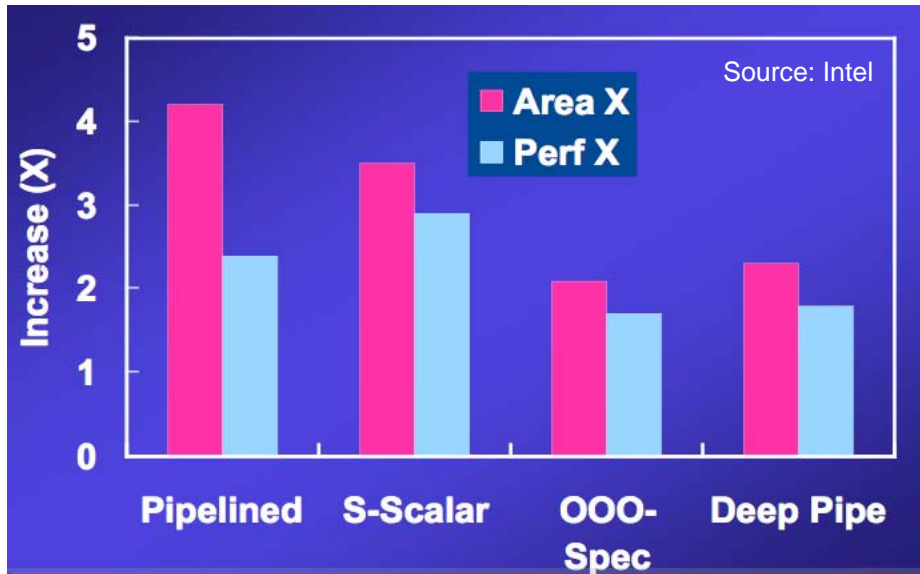
Trend in Microprocessor Performance

Goal: 10 TIPS by 2015

How to get there ?



But, What About Area & Power Efficiency?



Computation Power / # Transistors & Frequency ↘ !!

Example	ARM2	Pentium P4
$\frac{\# \text{Instructions}/s}{\# \text{Tors} \times \text{Clockfreq}}$	$\frac{4 \times 10^6}{(3 \times 10^4) \times (8 \times 10^6)} \approx 1.3 \times 10^{-4}$	$\frac{10^{10}}{(10^8) \times (2 \times 10^9)} \approx 5 \times 10^{-8}$

A New Set of Paradigms are Emerging

- Move away from the Basic “Frequency & Size” Rationales
- From “100% Correct” to “Less than Perfect” Circuits
- Resilience Achieved via Application of Redundancy Techniques wrt to Manufacturing Defects and Transient Faults
- Static and On-line Degradable-Reconfigurable Circuits (Memory)
- From “X-Scalar” to “Vectorial” Multi-Core Processor Architectures

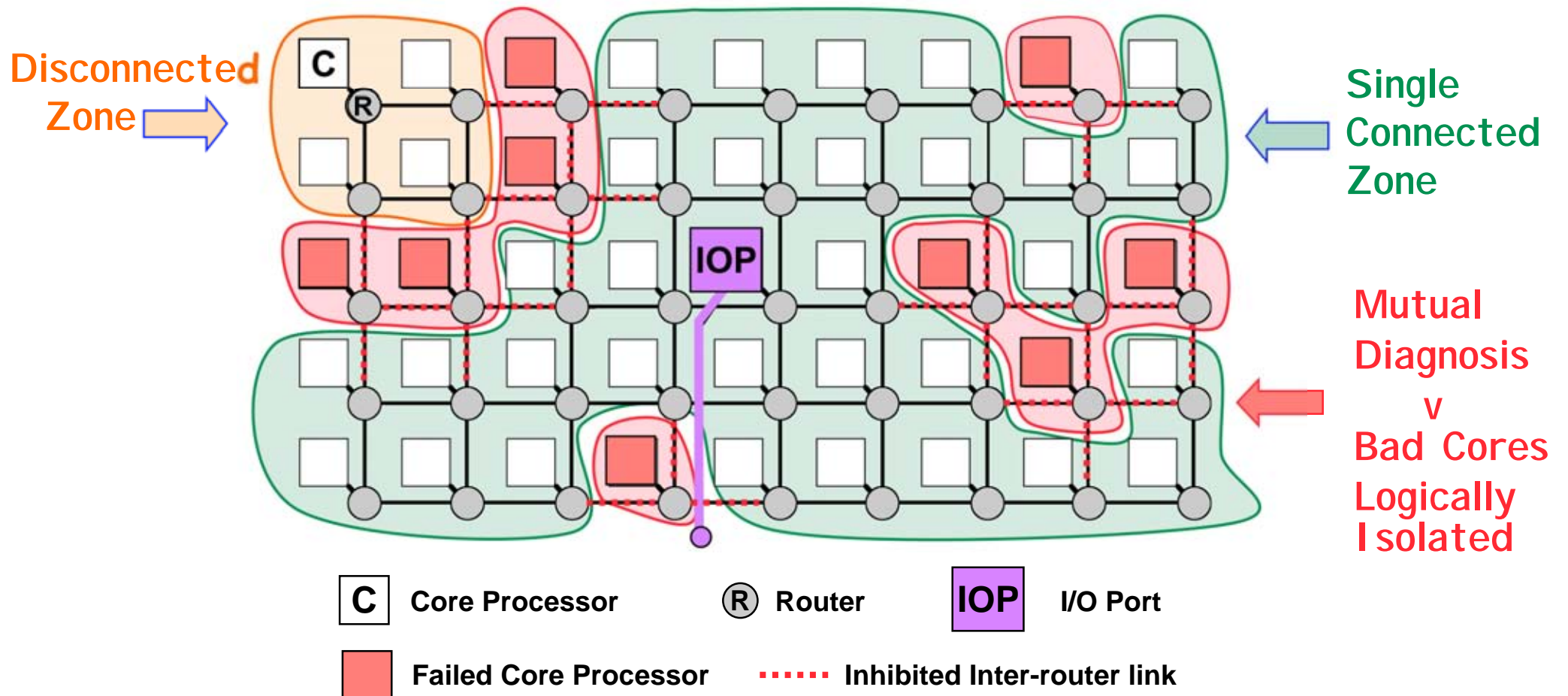
From Multi-Cores Architectures To Multi-Multi-Cores Architectures



- Multi-Core: ↗ performance while coping with power dissipation issues (very high clock frequency)
- Still, ↘ transistor size for including many of such cores
—> significant % of defective cores (more than 10%)
- Current context:
 - ◆ Chips are sorted according to frequency
 - ◆ Single core processor = “Downgraded” dual core circuits ...
- How to go further?
Our proposal: **On-line reconfiguration to cope with faults**

Example Target Architecture

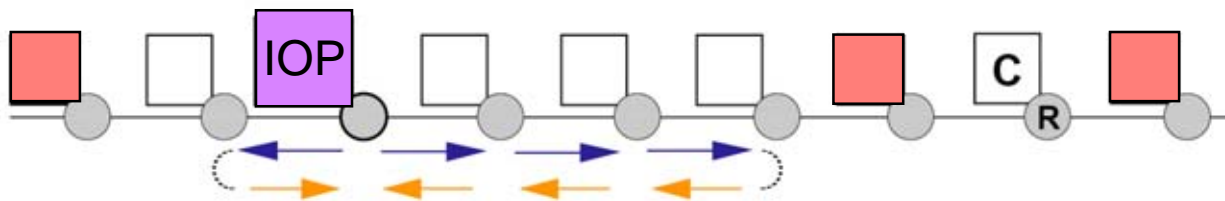
(5x9-node Network — Connectivity: 4)



Routing and Simulation

■ Self-configuration of Communications: Contract Net Protocol

- **Step 1:** The IOP broadcasts a **Request Message** across the Single Connected Zone (flooding, possibly inside a propagation radius). Each core adds the route to each forwarded message.
- **Step 2:** Each core sends an **Acknowledgement Message** to the IOP, which follows the RM route in the opposite direction.
- **Step 3:** The IOP stores the discovered routes in a special buffer (**Valid Route Buffer**).

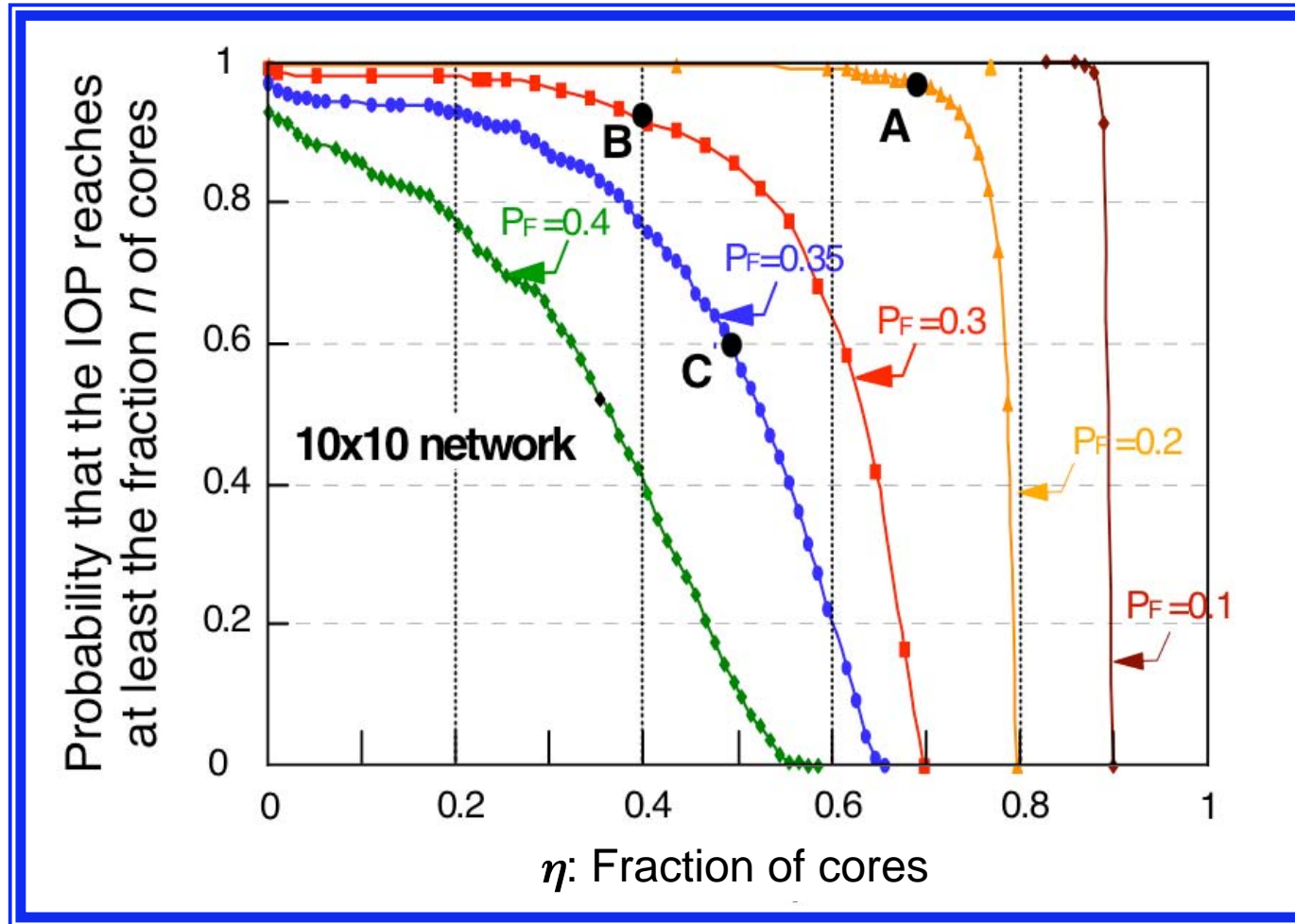


- 1: *Request Message*
- 2: *Acknowledgement Message*

■ Analysis of the Efficiency of the Protocol

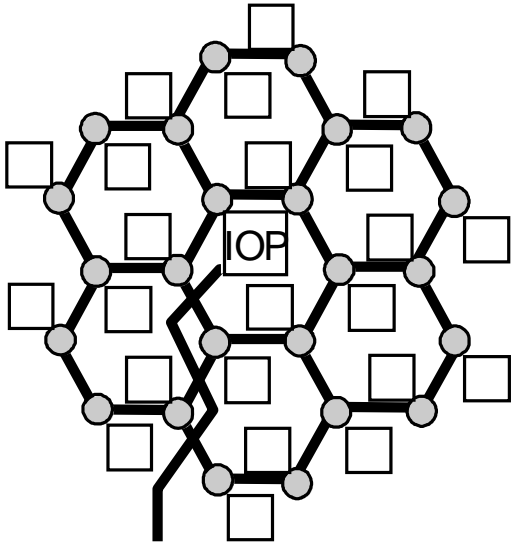
- ◆ **Simulation** of target architectures and topologies
- ◆ **MASS**: Multi Agent Software Simulator — <http://www.laas.fr/~collet>

Example of Results

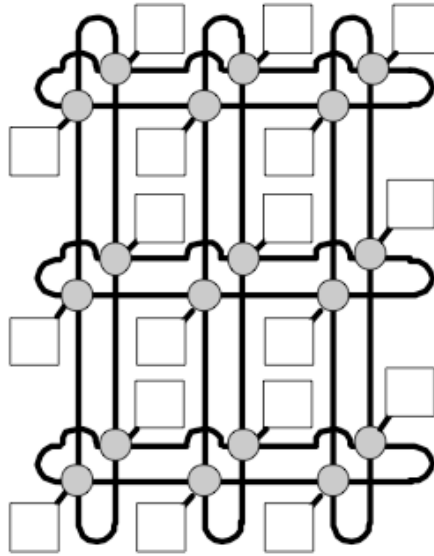


Point A ($X_A = 0.68$ and $Y_A = 0.96$) : the probability is approximately $Y_A = 0.96$ that the IOP reaches at least $\eta = 68\%$ of all cores when the core probability of failure $P_F = 0.2$.

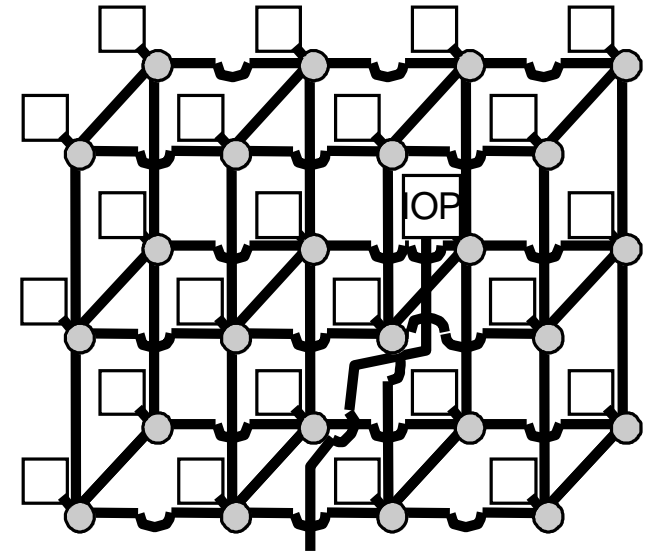
Other Possible Architectures



Hexagonal Net
(C=3, 24 nodes)

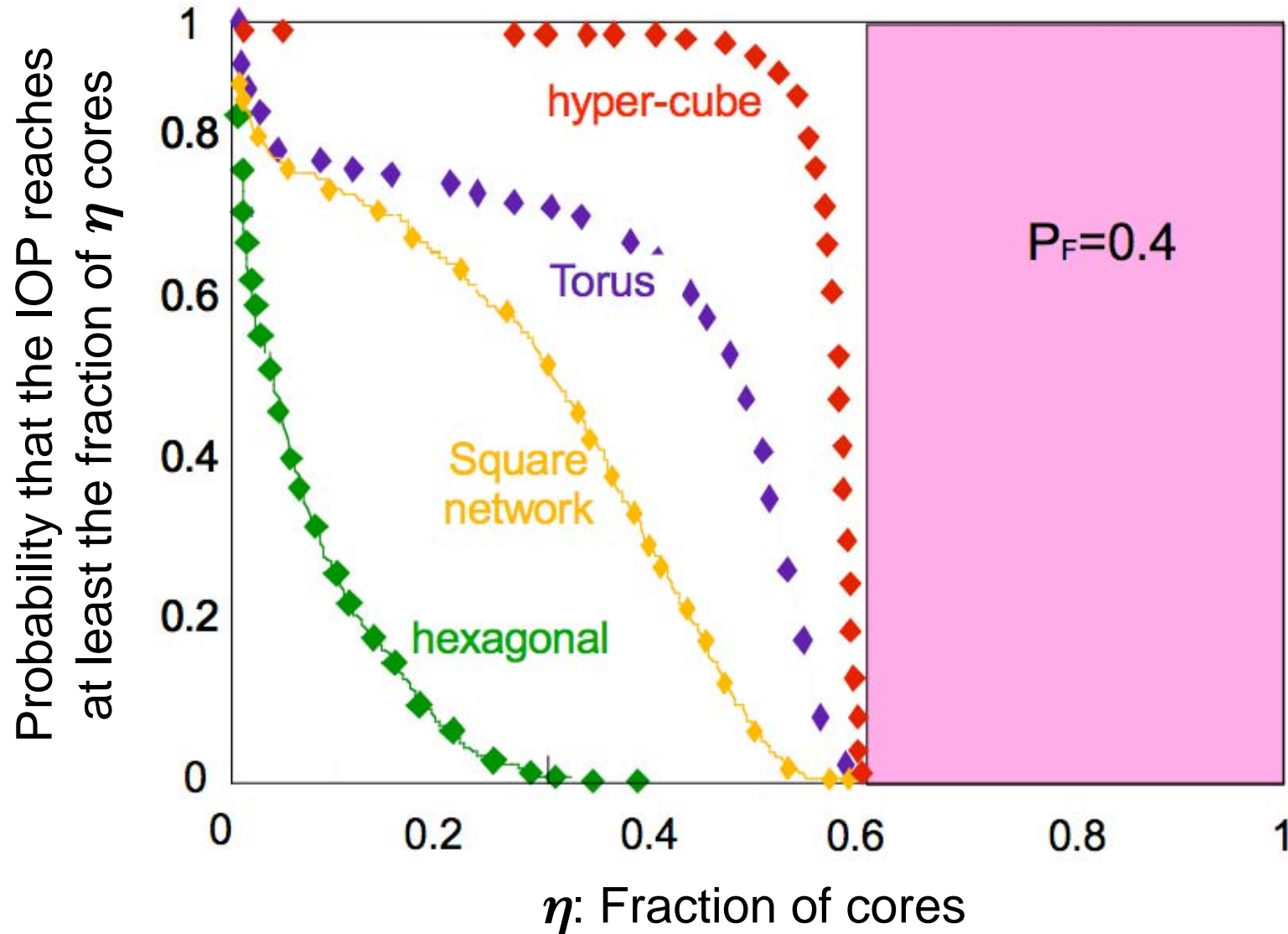


Torus
(C=4, 28 nodes)



Hypercube
(C=5, 24 nodes)

Impact of connectivity (\approx 450-node Networks)



Concluding Remarks

- The problems at stake are very challenging!
- Massively defective ICs including high % of “crummy” components are to be expected in any case — *top-down vs. bottom-up tracks* (see next slide)
- A “novel” perspective is thus emerging ... using the seminal ideas by:
 - Moore — not the same one :-) — & Shannon*
 - von Neumann**—> Old recipes — and much more — are back!
- A good opportunity for our community
- Keep our fingers crossed that SW technology catches up ...

* E.F. Moore, C.E. Shannon, Reliable Circuits Using Less Reliable Relays, *J. Franklin Institute*, pp. 181-208, 281-297, 1956

** J. Von Neumann, Probabilistic Logics and the Synthesis of Reliable Organisms from Unreliable Components, *Automata Studies*, C.E. Shannon, J. McCarthy, Eds., pp. 43-98, 1955

A Two-way Track...

- **“More Moore”**: The Evolutionary Path... (top-down)
Keep decreasing elementary device (silicon transistor) size
—> Increasing Effect of Variations: Dopants, Threshold, Temperature, Delay, Low Signal Strength, etc.
- **“More than Moore”**: The Revolutionary Path... (bottom-up)
Self-assembly of elementary devices in molecular electronics
—> Many Major Open Issues: Signal amplification, Selective Control of Transistors, Cascading, Scalability, etc.



**Nanoscale devices are inherently unreliable ...
and unpredictable!**

References and Future Work

■ To probe further

- ◆ P. Zajac, J. H. Collet, J. Arlat, Y. Crouzet, "Resilience through Self-Configuration in Future Massively Defective Nanochips", IEEE/IFIP DSN2007 - Supplemental Volume, Edinburgh, Scotland, UK, pp.266-271, June 28, 2007.
- ◆ P. Zajac, J. H. Collet, "Production Yield and Self-Configuration in the Future Massively Defective Nanochips", 22nd IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems, Roma, Italy, pp.197-205, Sept. 26-28, 2007.

■ On-going research

- ◆ IOP bottleneck and hardcore
- ◆ Mitigation of performance and dependability issues